

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Listing of Claims

1 1. (Currently Amended) A computerized method for selecting cells in a
2 circuit design database, the circuit design database having one or more levels of hierarchy
3 including one or more logic functions composed of one or more other logic functions
4 and/or one or more leaf cells, the leaf cells forming the lowest level of hierarchy in the
5 circuit design database, each of the leaf cells having one or more inputs and one or more
6 outputs, the circuit design database having one or more nets, each of the nets for
7 connecting an output port of a source leaf cell to an input port of one or more destination
8 leaf cells, the computerized method comprising the steps of:

9 selecting one of the nets via a user input device;

10 identifying selected leaf cells that are connected to the selected net, wherein the
11 selected leaf cells identified by the identifying step include only the source leaf cell that
12 is connected to the selected net; and

13 selecting the identified leaf cells.

1 2. (Original) A method according to claim 1, wherein the selected leaf
2 cells identified by the identifying step include all of the leaf cells that are connected to the
3 selected net.

1 3. (Canceled)

1 4. (Canceled)

1 5. (Original) A method according to claim 1, wherein each of the leaf
2 cells in the circuit design database is either placed or unplaced, the identifying step only
3 identifying those leaf cells that are connected to the selected net and are placed.

1 6. (Original) A method according to claim 1, wherein each of the leaf
2 cells in the circuit design database is either placed or unplaced, the identifying step only
3 identifying those leaf cells that are connected to the selected net and are unplaced.

1 7. (Currently Amended) ~~A method according to claim 1, further comprising~~
2 ~~the step of~~ A computerized method for selecting cells in a circuit design database, the
3 circuit design database having one or more levels of hierarchy including one or more
4 logic functions composed of one or more other logic functions and/or one or more leaf
5 cells, the leaf cells forming the lowest level of hierarchy in the circuit design database,
6 each of the leaf cells having one or more inputs and one or more outputs, the circuit
7 design database having one or more nets, each of the nets for connecting an output port of
8 a source leaf cell to an input port of one or more destination leaf cells, the computerized
9 method comprising the steps of:

10 selecting one of the nets via a user input device;

11 identifying selected leaf cells that are connected to the selected net;

12 selecting the identified leaf cells; and

13 setting a current context.

1 8. (Original) A method according to claim 7, wherein the selected leaf
2 cells identified by the identifying step include only those leaf cells that are connected to
3 the selected net and are in the current context.

1 9. (Original) A method according to claim 7, wherein the selected leaf
2 cells identified by the identifying step include only the source leaf cell that is connected
3 to the selected net and is in the current context.

1 10. (Original) A method according to claim 7, wherein the selected leaf
2 cells identified by the identifying step include only the destination leaf cells that are
3 connected to the selected net and are in the current context.

1 11. (Original) A method according to claim 7, wherein each of the leaf
2 cells in the circuit design database is either placed or unplaced, the identifying step only
3 identifying those leaf cells that are connected to the selected net, are placed, and are in
4 the current context.

1 12. (Original) A method according to claim 11, wherein the identifying
2 step only identifies the source leaf cell that is connected to the selected net, is placed, and
3 is in the current context, if any.

1 13. (Original) A method according to claim 11, wherein the identifying
2 step only identifies the source leaf cell that is connected to the selected net, is unplaced,
3 and is in the current context, if any.

1 14. (Original) A method according to claim 7, wherein each of the leaf
2 cells in the circuit design database is either placed or unplaced, the identifying step only
3 identifying those leaf cells that are connected to the selected net, are unplaced, and are in
4 the current context.

1 15. (Original) A method according to claim 1, wherein two or more of the
2 nets are selected, and the identifying step identifies selected leaf cells that are connected
3 to any of the selected nets.

1 16. (Original) A method according to claim 15, wherein the identifying
2 step identifies only those leaf cells that are placed.

1 17. (Original) A method according to claim 15, wherein the identifying
2 step identifies only those leaf cells that are unplaced.

1 18. (Original) A method according to claim 15, wherein the identifying
2 step identifies only those leaf cells that are in a current context.

1 19. (Original) A method according to claim 15, wherein the identifying
2 step identifies only those leaf cells that are source leaf cells for the selected nets.

1 20. (Original) A method according to claim 15, wherein the identifying
2 step identifies only those leaf cells that are destination leaf cells for the selected nets.

1 21. (Currently Amended) ~~A method according to claim 15~~ A computerized
2 method for selecting cells in a circuit design database, the circuit design database having
3 one or more levels of hierarchy including one or more logic functions composed of one
4 or more other logic functions and/or one or more leaf cells, the leaf cells forming the
5 lowest level of hierarchy in the circuit design database, each of the leaf cells having one
6 or more inputs and one or more outputs, the circuit design database having one or more
7 nets, each of the nets for connecting an output port of a source leaf cell to an input port of
8 one or more destination leaf cells, the computerized method comprising the steps of:
9 selecting two or more of the nets via a user input device, wherein the two or more
10 nets are part of a vectored net;
11 identifying selected leaf cells that are connected to any of the selected nets;
12 selecting the identified leaf cells.

1 22. (Original) A method according to claim 21, wherein the vectored net
2 is selected at an interface of a selected logic function.

1 23. (Currently Amended) A computerized method for selecting and aligning
2 cells in a circuit design database using a placement tool, the circuit design database
3 having one or more levels of hierarchy including one or more logic functions composed
4 of one or more other logic functions and/or one or more leaf cells, the leaf cells forming
5 the lowest level of hierarchy in the circuit design database, each of the leaf cells having
6 one or more inputs and one or more outputs, the circuit design database having one or
7 more nets, each of the nets for connecting an output port of a source leaf cell to an input
8 port of one or more destination leaf cells, the computerized method comprising the steps
9 of:

10 selecting one or more of the nets via a user input device;
11 identifying and selecting selected leaf cells that are connected to the selected one
12 or more nets, wherein the selected leaf cells identified by the identifying step include
13 only the source leaf cell(s) that are connected to the one or more selected nets;
14 identifying an alignment axis; and
15 aligning selected ones of the identified leaf cells in the direction of the alignment
16 axis.

1 24. (Original) A method according to claim 23, wherein the alignment
2 axis is substantially horizontal.

1 25. (Original) A method according to claim 23, wherein the alignment
2 axis is substantially vertical.

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1 26. (Original) A method according to claim 23, wherein each of the leaf
2 cells in the circuit design database is either placed or unplaced, the aligning step further
3 including the step of placing the identified leaf cells if not already placed.

1 27. (Original) A method according to claim 26, wherein the unplaced
2 identified leaf cells are first placed in a predetermined region before alignment.

1 28. (Original) A method according to claim 23, wherein the aligning step
2 puts the selected identified leaf cells into a predetermined order along the alignment axis.

1 29. (Original) A method according to claim 28, A computerized method
2 for selecting and aligning cells in a circuit design database using a placement tool, the
3 circuit design database having one or more levels of hierarchy including one or more
4 logic functions composed of one or more other logic functions and/or one or more leaf
5 cells, the leaf cells forming the lowest level of hierarchy in the circuit design database,
6 each of the leaf cells having one or more inputs and one or more outputs, the circuit
7 design database having one or more nets, each of the nets for connecting an output port of
8 a source leaf cell to an input port of one or more destination leaf cells, the computerized
9 method comprising the steps of:

10 selecting one or more of the nets via a user input device, wherein the one or more
11 nets are part of a vectored net having ordered bits;
12 identifying and selecting selected leaf cells that are connected to the selected one
13 or more nets;

14 identifying an alignment axis; and
15 aligning selected ones of the identified leaf cells in the direction of the alignment
16 axis, wherein the aligning step puts the selected identified leaf cells into a predetermined
17 order along the alignment axis.

1 30. (Original) A method according to claim 29, wherein the aligning step
2 orders the selected identified leaf cells in accordance with the ordered bits of the vectored
3 net.

1 31. (Original) A method according to claim 29, wherein the aligning step
2 orders the selected identified leaf cells in reverse of the ordered bits of the vectored net.

1 32. (Original) A method according to claim 29, wherein each of the
2 identified leaf cells is associated with one of the ordered bits of the vectored net, and the
3 identified leaf cells for each ordered bit has one source leaf cell and at least one
4 destination leaf cell, the aligning step putting the source leaf cells into a predetermined
5 order along the alignment axis, and putting the at least one destination leaf cell adjacent
6 the corresponding source leaf cell along an axis that is perpendicular to the alignment
7 axis.

1 33. (Original) A data processing system for selecting cells in a circuit
2 design database, the circuit design database having one or more levels of hierarchy
3 including one or more logic functions composed of one or more other logic functions

4 and/or one or more leaf cells, the leaf cells forming the lowest level of hierarchy in the
5 circuit design database, each of the leaf cells having one or more inputs and one or more
6 outputs, the circuit design database having one or more nets, each of the nets for
7 connecting an output port of a source leaf cell to an input port of one or more destination
8 leaf cells, the data processing system comprising:

9 net selection means for selecting one or more of the nets of the circuit design
10 database;

11 leaf cell identifying means for identifying selected leaf cells that are connected to
12 the selected net(s), wherein the selected leaf cells identified by the identifying means
13 include only the source leaf cell(s) that is/are connected to the selected net(s); and

14 leaf cell selecting means for selecting the identified leaf cells.

1 34. (Original) A data processing system according to claim 33, further
2 comprising:

3 identifying means for identifying an alignment axis; and

4 aligning means for aligning the identified leaf cells in the direction of the
5 alignment axis.

6

7 35. (New) A computerized method for selecting cells in a circuit design
8 database, the circuit design database having one or more levels of hierarchy including one
9 or more logic functions composed of one or more other logic functions and/or one or
10 more leaf cells, the leaf cells forming the lowest level of hierarchy in the circuit design
11 database, each of the leaf cells having one or more inputs and one or more outputs, the

12 circuit design database having one or more nets, each of the nets for connecting an output
13 port of a source leaf cell to an input port of one or more destination leaf cells, the
14 computerized method comprising the steps of:
15 selecting one of the nets via a user input device;
16 identifying selected leaf cells that are connected to the selected net, wherein the
17 selected leaf cells identified by the identifying step only include one or more of the
18 destination leaf cell(s) that is/are connected to the selected net; and
19 selecting the identified leaf cells.

1 36. (New) A computerized method for selecting and aligning cells in a circuit
2 design database using a placement tool, the circuit design database having one or more
3 levels of hierarchy including one or more logic functions composed of one or more other
4 logic functions and/or one or more leaf cells, the leaf cells forming the lowest level of
5 hierarchy in the circuit design database, each of the leaf cells having one or more inputs
6 and one or more outputs, the circuit design database having one or more nets, each of the
7 nets for connecting an output port of a source leaf cell to an input port of one or more
8 destination leaf cells, the computerized method comprising the steps of:
9 selecting one or more of the nets via a user input device;
10 identifying and selecting selected leaf cells that are connected to the selected one
11 or more nets, wherein the selected leaf cells identified by the identifying step only
12 include one or more of the destination leaf cell(s) that is/are connected to the one or more
13 selected net;
14 identifying an alignment axis; and

15 aligning selected ones of the identified leaf cells in the direction of the alignment
16 axis.

1 37. (New) A data processing system for selecting cells in a circuit design
2 database, the circuit design database having one or more levels of hierarchy including one
3 or more logic functions composed of one or more other logic functions and/or one or
4 more leaf cells, the leaf cells forming the lowest level of hierarchy in the circuit design
5 database, each of the leaf cells having one or more inputs and one or more outputs, the
6 circuit design database having one or more nets, each of the nets for connecting an output
7 port of a source leaf cell to an input port of one or more destination leaf cells, the data
8 processing system comprising:

9 net selection means for selecting one or more of the nets of the circuit design
10 database;

11 leaf cell identifying means for identifying selected leaf cells that are connected to
12 the selected net(s), wherein the selected leaf cells identified by the identifying means only
13 include one or more of the destination leaf cell(s) that is/are connected to the one or more
14 selected net(s); and

15 leaf cell selecting means for selecting the identified leaf cells.